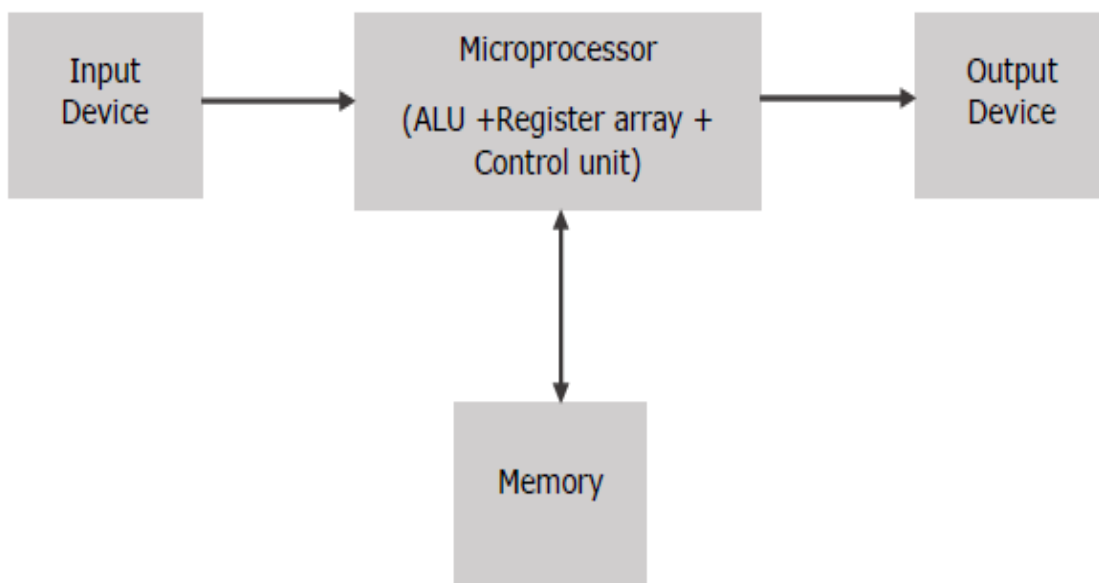


UNIT- 1

MICROPROCESSOR AND ITS INTERFACE

- The processor of a micro-computer is called microprocessor.
- It is a programable logical device which takes data as input and process the data according to the instruction given and gives output .
- Micro computers is a very small computer assembled to do a specific task.

BLOCK DIAGRAM OF A MICROPROCESSOR COMPUTER



BLOCK DIAGRAM OF A MICROPROCESSOR



ALU:- Arithmetic and logical unit

- It performs all kinds of arithmetic and logical operation according to the instruction and data given to it .

Register Array:-

- Register stores data
- Register array means group of registers
- It stores input data and result for temporary period to be used by the ALU .

Control Unit :-

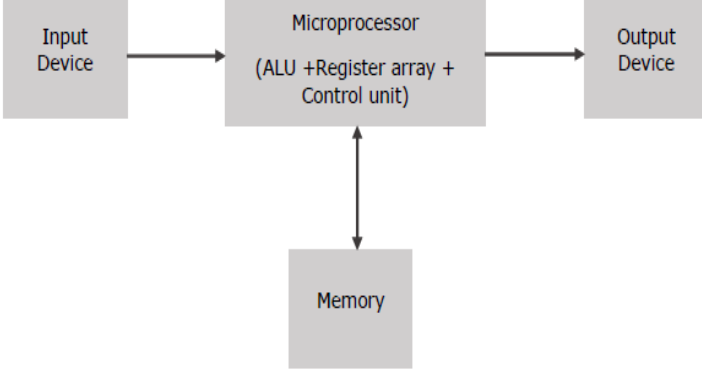

- It gives the control signal to the ALU and register array so that all the works are done in the proper co-ordination

Application of Microprocessor:-

- Domestic Application

- Industrial Application
- Automobiles Application
- Packing Industries application
- In robotics

Difference between microcomputer and microprocessor

Micro-Computer	Microprocessor
<ul style="list-style-type: none"> • Microcomputer is a very small computer assembled to do a specific task . 	<ul style="list-style-type: none"> • The processor of a microcomputer is called microprocessor 
<ul style="list-style-type: none"> • Micro-computer is a system 	<ul style="list-style-type: none"> • Microprocessor is a component of the system

Evolution of microprocessor:-

- In 1971, Intel corporation of USA developed first microprocessor called "Intel 4004".
- It was unit processor that means at a time 4 bits of data could be handled by the processor.

- In the year 1971 again another 4 bit processor was developed named “**Intel 4040**”
- In 1972 first 8 bit processor was developed by Intel corporation named “**Intel 8008**”. It was using P-MOS technology. So the speed was very low.
- In 1973 another 8 bit processor was developed by Intel corporation named “**Intel 8080**”. It was faster because N-MOS technology was used.
- In 1975 one very successful 8-bit processor was developed by Intel corporation named “**Intel 8085**”. It was using N-MOS technology and single power supply.
- 1978, first 16 bit processor was developed named “**Intel 8086**”
- In subsequent years many other companies took to develop microprocessor, such as zilogs, Motorola ,Celeron, Fairchild etc.
- The other 16 bit processors are **80186, 80286, 80386, 80486** etc. 280, 2800, PI, PII, PIII, PIV etc
- After successful development of 16 bit processor 32 bit processor was developed by many companies.
- Latest in market 64 bit processor are using this i-series such as **i3, i5, i7, i9**.

Word Length :-

- The data handling capacity of any processor is called word length of processor.
- Example:- Intel 8085 is a 8 bit processor. So its wordlength is = 8 bit
- Intel 4004 is a 4 bit processor so its wordlength is = 4 bit.

UNIT-2

Intel 8085:-

Special features of Intel 8085:-

- It is a 8 bit processor.
- It uses N-MOS technology.
- It has 40 pins.
- It is a DIP chip (Dual in-line package).
- It uses frequency of 3mHz.
- It has a clock duration of 330 nsec.

$$\frac{1}{3\text{mhz}} = \frac{1}{3 \times 10^2} = \frac{10^{-6}}{3} = \frac{1}{3} * 10^{-6}$$

$$= 0.33 \times 10^{-6} \text{ sec}$$

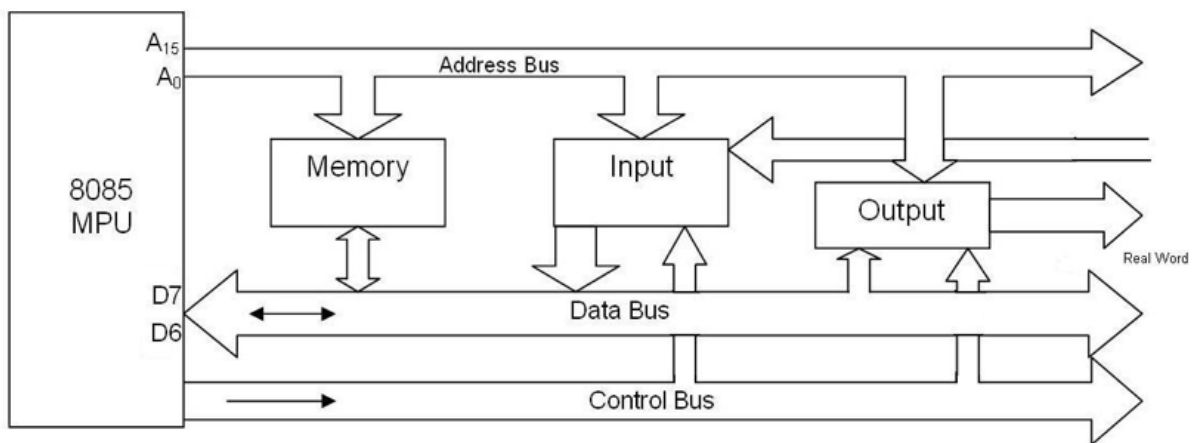
$$= 330 \text{ Nano second}$$

- It uses +5v power supply.

BUS ARCHITECTURE OF INTEL 8085

BUS:-

- In a processor bus means no. of parallel line used for the transportation of address, data and control signals
- This transportation is done from the processor to the I/O device and memories
- There are 3 kinds of buses in Intel 8085.
 - Address bus
 - Data bus
 - Control bus



a) Address bus:-

- It is used to carry the address of a particular location in memory or I/O device.
- In intel 8085, the address bus is of 16 bit circle
- It can allocate 64KB of memory location.
 - $\Rightarrow 2^{16} = 2^{10} * 2^6$ ($2^{10} = 1\text{KB}$)
 - $\Rightarrow 64 \times 1 \text{ KB} = 64 \text{ KB}$.
- The size of address bus gives the information of memory allocation capacity.

- The address line of address bus starts with A_0 and finishes with A_{15} .
- The address bus is unidirectional.

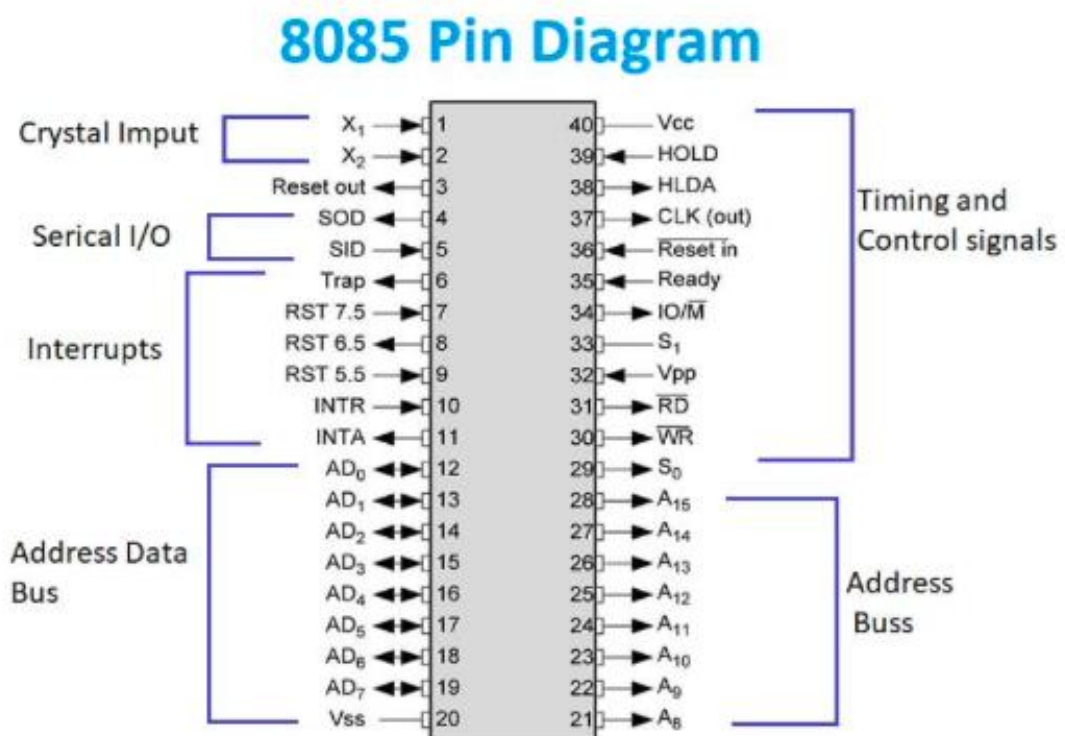
b) Data bus:-

- The data bus carries the data from processes to I/O devices and memory
- In Intel 8085 the data bus is 8 bit wide i.e. D_0 to D_7 .
- The data bus size gives the information of data handling capacity or word length of the processor
- The data bus is always bi-directional.

c) Control bus:-

- This is also unidirectional
- It carries the control signals for data address bus.

PIN CONFIGURATION OF INTEL 8085



Multiplexing:-

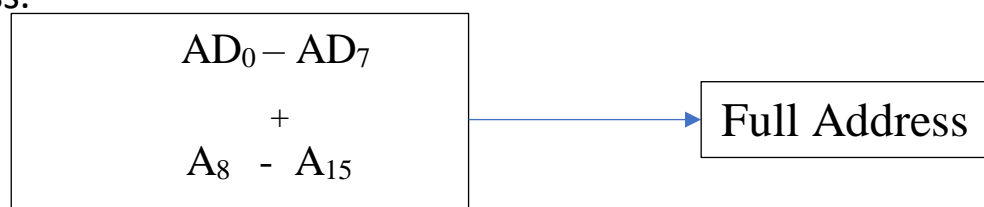
- The address bus size is 16 bit wide i.e. A_0 to A_{15} and data bus size is 8 bit wide i.e. D_0 to D_7 .
- The total address bus can be divided into 2 groups i.e. lower order address bus A_0 to A_7 higher order address bus A_8 to A_{15}
- In multiplexing the lower order address bus is mixed with data bus to AD bus.
- This is done to reduce the number of pins in the chip.

$AD_0 - AD_7$:-

- These pins are bidirectional pins
- These are address and data bus lines
- Through these pins lower order address as well as data go.

$A_8 - A_{15}$:-

- These are output pins
- These pins carry higher order address
- The lower order address goes through AD bus and higher order address goes through $A_8 - A_{15}$, they combine and make the full address.



ALE (Address latch Enable) :-

- This is an output pin
- When this pin goes high, the lower order address is mixed with higher order address and finally the data goes from the AD bus to the memory location.

$\overline{IO/\overline{M}}$

- This is an output pin

- When this pin goes high the processor is communicating with IO device using its buses.
- But when this pin goes low processor is communicating with memory.

\overline{RD}

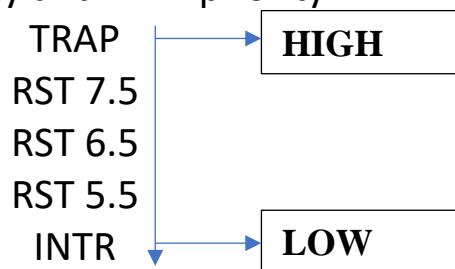
- This is a output pin.
- This is an active low pin/signal.
- When these pin. Goes low the processor reads the data from IO device or memory

\overline{WR}

- It is an output pin
- This is an active low pin/signal
- When these pin goes low the processor writes the data into the I/O device or memory.

TRAP, RST 7.5, 6.5, 5.5, INTR:-

- Interruption means disturbing the processor for a short duration.
- In Intel 8085 there are 5 interrupt lines, they are TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR
- All these are active high pins
- TRAP has the highest priority and INTR priority



- These are all input pins
- The interrupt which can be avoided are called maskable interrupts those are RST 7.5, RST 6.5, RST 5.5 AND INTR
- Those interrupts which cannot be avoided are called non-maskable interrupt, i.e. TRAP is the non – maskable interrupt.

INTA;- (Interrupt acknowledgement)

- It is an output pin.
- It is an active low signal
- When this pin goes low, the processor tells that it has received and interrupt request

HOLD :-

- This is an input pin, when this is high, the external devices request to the processor for the use of busses (address bus and data bus)

HLDA:-

- It stands for HOLD Acknowledgement
- When this pin goes high processor tells that, it has received the whole request and the control over the busses is given to the device as soon as the current work is complete.

RESET IN

- This is an input and active low pin
- It resets the PC 20 and it also resets interrupt enable lines and HLDA flip flops.

RESET OUT:-

- It is an output and active high pin
- When this goes high the CPU is in reset condition

X₂ & X₂:-

- These are external terminals connected to the crystal oscillator to produce a suitable clock for the operation of microprocessor.

SOD:-

Serial Output Data

- The 7th bit of the accumulator is placed on SOD line

SID:-

- It is a data line for serial input
- the data on this line is loaded into the 7th bit of the accumulator.

READY:-

- It is an input pin and It is used by the processor to sense whether the peripheral is ready or not for the data transfer.

S₀ & S₁:-

- These are status signals to let the users know that a processor is doing what kind of work.

S ₁	S ₀	
0	0	HLT
0	1	WRITE
1	0	READ
1	1	FETCH

+V_{CC}:-

- 5V Supply

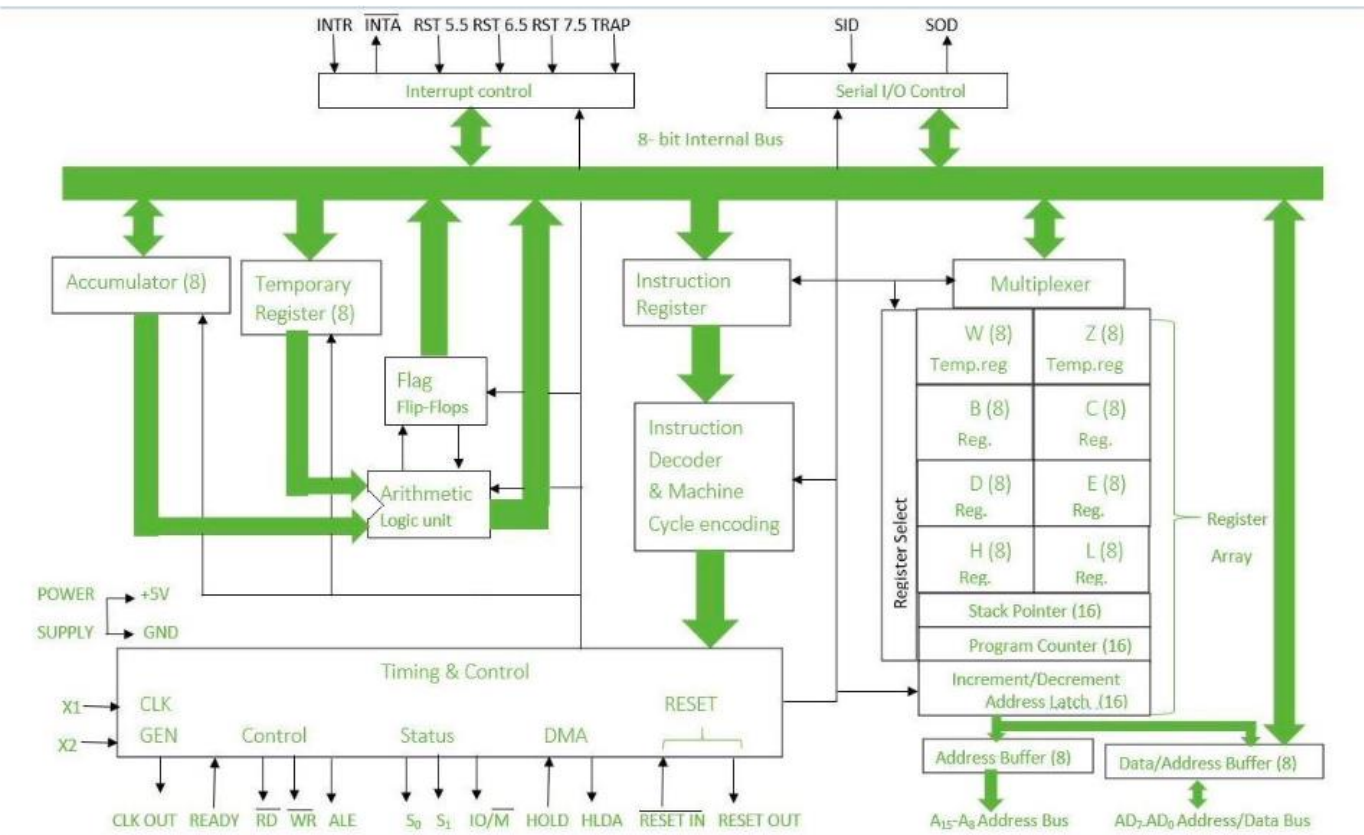
Clk (out):-

- Clock signal

V_{SS}:-

- Ground

INTERNAL ARCHITECTURE OF INTEL 8085



- The internal architecture of Intel 8085 gives the idea of basic blocks or units present.

Accumulator:-

- It is an important register of the processor because all the data from memory goes to accumulator first also after processing the result also stored in accumulator.
- It is a 8-bit register that means it can store 8-bit of data only.
- It is denoted by 'A'.

Register Organisation:-

- There are many registers present in INTEL 8085. Broadly, we can divide the registers in 2 groups:-
 - i) General purpose register (GPR).
 - ii) Special purpose register (SPR).

GPR:-

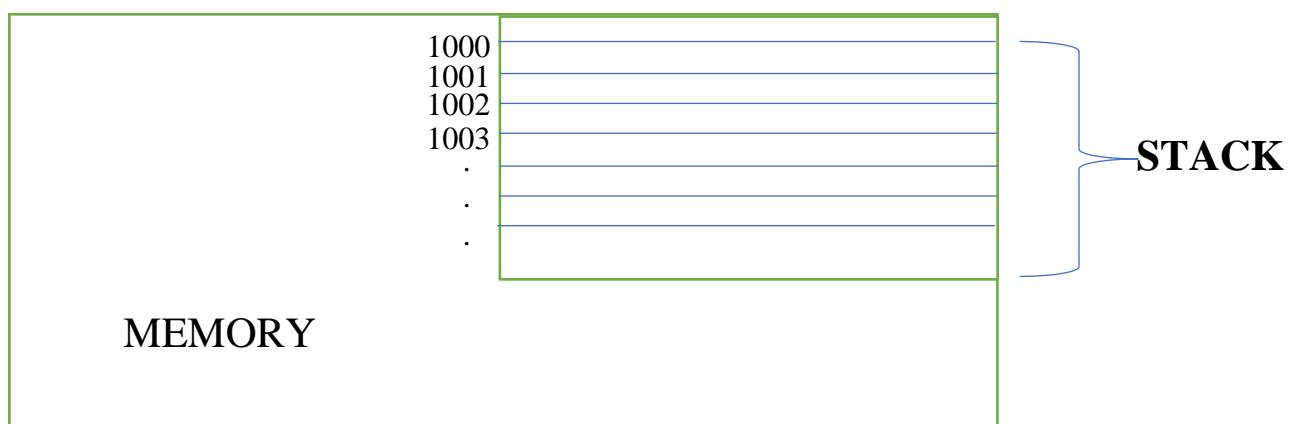
- There are 6 GPRs present in INTEL 8085. They are :- B, C, D, E, H, L.
- All GPRs are of 8 bit i.e. they can store 8 bits of data only
- To store 16 bit data using GPRs pairing can be done, pairing means joining 2 GPRs.
- In INTEL 8085 the register pairs are B-C, D-E, H-L.
- All pairs are of 16 bit size
- Among all the pairs H-L pair is the most important one because it is used for memory allocation

SPR:-

- There are 4 SPRs present in INTEL 8085. They are:-
 - i) Stack pointer (SP)
 - ii) Program Counter (PC)
 - iii) Instruction Register (IR)
 - iv) Temporary Register (TR)

STACK POINTER:-

- It is a 16 bit register
- STACK:- It is a portion of whole memory.
- In stack there are few locations where the data is stored temporarily, which is used while writing a program
 - The top most location of the stack is called STACK TOP.



- SP or stack pointer stores the address of the stack top. For example:- Stack pointer stores 1000

Program counter (PC):-

- This register stores the address of next instruction to be executed while writing a program.
- It is a 16-bit register.

Instruction register:-

- It stores the decoded form of instruction while writing a program.
- It is also a 16-bit register

Temporary register:-

- It is a 8 bit register and stores the data for a very short period while writing a program.

Status FCAG:-

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
S	Z	X	AC	X	P	X	Cy

- It is a 8 bit register whose bit pattern is shown in the fig. above.
- The status bit in the register are:-
 - i) Carry (Cy)
 - ii) Parity (P)
 - iii) Auxiliary carry (AC)
 - iv) Zero (Z)
 - v) Sign (s)

I. Carry:-

After the execution of arithmetic operation, if there is a carry then (Cy) = 1 & if there is no carry then Cy = 0.

II. Parity:-

In arithmetic operation output if no. 1's is even then p = 1, if no. of 1's is odd then p = 0.

III. Auxiliary carry :-

If the O/P of arithmetic operation has a carry from 3rd bit to 4th bit then AC = 1 and if there is no carry from 3rd bit to 4th bit then AC = 0

IV. Zero:-

If the arithmetic result is zero then Z = 1, if the result is non zero then Z = 0.

V. Sign:-

If arithmetic result is negative (-) then S = 1 otherwise S = 0.

E.g. **Q. Add 23H and 11H.**

Ans:-

$$\begin{array}{r}
 23H \quad 0010 \quad 0011 \\
 11H \quad 0001 \quad 0001 \\
 \hline
 34H \quad 0011 \quad 0100 \\
 \text{Cy} = 0, \text{ P} = 0, \text{ AC} = 0, \text{ Z} = 0, \text{ S} = 0
 \end{array}$$

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	0	0	0	0

So, the flag bit is 00H.

Timing and control unit:-

- It is the brain of computer
- It provides necessary timing and control signal to all the operations which are required during execution of program.
- It controls the flow of data between the processor and its peripheral. (I/O device).

I/O device:-

- User can enter the instruction and data into the memory through I/O devices.
- Microprocessor reads the instructions from memory, processes the data according to the instructions given.
- Result is displayed in the O/P devices.

UNIT – 3

Instruction:-

Instruction is a set of commands to do a specific task.

Instruction set:-

- It is a group of instructions.
- The instructions set in INTEL 8085 are classified into 5 groups they are:-
 - i) Data transfer group
 - ii) Arithmetic group
 - iii) Logical group
 - iv) Branch control group
 - v) Machine and I/O control group

a) Data transfer group:-

- MOV r_1, r_2 [The content of r_2 is moved to r_1]
 $[r_1] \leftarrow [r_2]$

E.g.

- i) MOV A, B
- ii) MOV B, A
- iii) MOV A, C
- iv) MOV C, A

- MOV r, m [The content of memory is moved to any GPR or A]
 $[r] \leftarrow [m]$

E.g.

- i) MOV A, M
- ii) MOV B, M
- iii) MOV C, M

- MVI $r, (data)_{8 \text{ bit}}$ [A 8 bit data is moved immediately to a register].

$$[r] \leftarrow [data]_{8 \text{ bit}}$$

E.g.

- i) MVI B, 32H

- ii) MVI C, 80H
- iii) MVI A, 00H

- LDA (addr.) [The content of memory address is loaded into the accumulator].

[A] ← [addr.]

E.g.

- i) LDA 1000H
- ii) LDA 2500H
- iii) LDA 3000H

- STA (addr.) [The content of accumulator is stored in memory address].

[addr.] ← [A]

E.g.

- i) STA 1000H
- ii) STA 2500H
- iii) STA 3000H

Q. Write a program to get 32H in register B, transfer the data in accumulator again transfer the data to register C. Also move the data to accumulator. Finally store the data in 200H.

Ans:-

```

MVI    B, 32H
MOV    A, B
MOV    C, A
MOV    A, C
STA    2000H
HLT

```

Q. Write a program to get a 8 bit data from memory location 1000H. Transfer the data to register B again transfer the data to register C. Also move the data to accumulator. Finally store the data in 2000H.

Ans:-

```

LDA    1000H [ The content of 1000H -> 32H
which   is moved to A]
MOV    B, A
MOV    C, B

```


STA 2000H
HLT

- LXI H, 16 bit data [Load the H-L pair with a 16 bit data, That 16 bit data -> add of memory location].
E.g. LXI H, 1250 H
- LHL D addr. [load the H-L pair directing with address locations]
- SHL D addr. [Store the H-L pair content into address locations]
- XCHG addr. [Exchange the H-L pair content to D-E pair]

Q. WAP to get number from 9000H move it to register B, store the number in 9001H.

Ans. LDA 9000H
MOV B, A
MOV A, B
STA 9001H
HLT

b) Arithmetic group:-

- ADD r [The content of register 'r' is added with acc content & the result is stored in 'A'].
 $[A] \leftarrow [r] + [A]$ E.g. ADD B
- ADI (data)_{8 bit} [The immediate 8 bit data is added with account content and the result is stored in 'A'].
 $[A] \leftarrow [A] + \text{data}$ E.g. ADI . 80_H
- ADD M [The content of memory location is added with account content & the result is stored in 'A'].
- SUB r [The content of register 'r' is subtracted from accumulator content and the result is stored in A].
 $[A] \rightarrow [A] - [r]$.
E.g. SUB c
- SUI (data)_{8 bit} [The immediate 8 bit data is subtracted from account content and the result is stored in 'A'].
- SUB M [The content of memory location is subtracted from account content and result is stored in A].
- INR r [increment the content of register by 1]

- E.g. INR B -> [B] <- [B] + 1
- DCR r [decrement the content of register by 1]
E.g. DCR C -> [C] <- [C] -1
 - INX rp [Increase the register pair by 1].
E.g. INX H (H-C)
INX D (D-E)
INX B (B-C)
 - DCX rp [decrement the register pair by 1]
E.g. DCX B
DCX D
DCX H
 - DAD D [The content of D-E pair is added with H-L pair and the result is stored in H-C Pair]
 - DAA [Decimal adjustment the account content].

Q. WAP to get 2 nos. from 9000H & 9001H location. Add the 2 nos. store the result in 9002H Location.

Ans. LDA 9000H
MOR B, A
LDA 9001H
ADD B → A + B → A
STA 9002H
HLT

C) Logical Group:-

OPCODE	OPERAND	DESTINATION	EXAMPLE
ANA	R	A = A AND R	ANA B
ANA	M	A = A AND Mc	ANA 2050
ANI	8-bit data	A = A AND 8-bit data	ANI 50
ORA	R	A = A OR R	ORA B
ORA	M	A = A OR Mc	ORA 2050

OPCODE	OPERAND	DESTINATION	EXAMPLE
ORI	8-bit data	A = A OR 8-bit data	ORI 50
XRA	R	A = A XOR R	XRA B
XRA	M	A = A XOR Mc	XRA 2050
XRI	8-bit data	A = A XOR 8-bit data	XRI 50
CMA	none	A = 1's compliment of A	CMA
CMP	R	Compares R with A and triggers the flag register	CMP B
CMP	M	Compares Mc with A and triggers the flag register	CMP 2050
CPI	8-bit data	Compares 8-bit data with A and triggers the flag register	CPI 50
RRC	none	Rotate accumulator right without carry	RRC
RLC	none	Rotate accumulator left without carry	RLC
RAR	none	Rotate accumulator right with carry	RAR
RAL	none	Rotate accumulator left with carry	RAR
CMC	none	Compliments the carry flag	CMC
STC	none	Sets the carry flag	STC

Q. WAP to get a 8 bit number from 9000H increment it by 1 then store it in 9001H.

Ans:-

```
LDA 9000H
INR A
STA 9001H
```

```

HLT.
LXI H, 9000H
MOV A, M
INR A
STA 9001H
HLT

```

Q. WAP to find 1's complement of a 8-bit number.

Ans.

```

LDA 9000H
CMA
STA 9001H
HLT
LXI H 9001H
MOV A, M
CMA
STA 9002H
HLT

```

Branch Group:-

OPCODE	OPERAND	EXPLANATION	EXAMPLE
JC	address	Jumps to the address if carry flag is 1	JC 2050
JNC	address	Jumps to the address if carry flag is 0	JNC 2050
JZ	address	Jumps to the address if zero flag is 1	JZ 2050
JNZ	address	Jumps to the address if zero flag is 0	JNZ 2050
JPE	address	Jumps to the address if parity flag is 1	JPE 2050

OPCODE	OPERAND	EXPLANATION	EXAMPLE
JPO	address	Jumps to the address if parity flag is 0	JPO 2050
JM	address	Jumps to the address if sign flag is 1	JM 2050
JP	address	Jumps to the address if sign flag is 0	JP 2050

Machine and I/O control group:-

- PUSH B [Here the content of register B goes to istack location]
- POP B [Here the content of stack goes to register B].
- OUT (Port Addr.)_{8-bit} [Here the content of account goes to port address].

E.g.